

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

WANG *et al.*

Appl. No.: To Be Assigned

Filed: Herewith (March 31, 2004)

For: **Hardware-Efficient
Implementation of Dynamic
Element Matching in Sigma-Delta
DAC's**

Confirmation No.: To Be Assigned

Art Unit: To Be Assigned

Examiner: To Be Assigned

Atty. Docket: 1875.3750001/RES/GSB

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final

Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of \$_____ in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of \$_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.
- ☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below:
- ☐ 7. Copies of the documents are submitted herewith.
- ☒ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. **10/354,159**, filed

January 30, 2003, which is relied upon for an earlier filing date under 35 U.S.C.

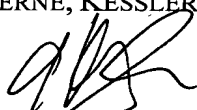
§ 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



George S. Bardmesser
Attorney for Applicants
Registration No. 44,020

Date: March 31, 2004

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Washington, D.C. 20005-3934
(202) 371-2600

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
1875.3750001/RES/GSBAPPLICATION NO.
To Be AssignedFIRST NAMED INVENTOR
Minsheng WANGFILING DATE
Herewith (March 31, 2004)ART UNIT
To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	US-5,305,004	04/1994	Fattaruso, John W.	341	120	
	AB1	US-5,404,142	04/1995	Adams et al.	341	144	
	AC1	US-6,124,813	09/2000	Robertson et al.	341	143	
	AD1	US-6,570,521	05/2003	Schofield, William G. J.	341	144	
	AE1	US-6,577,261	06/2003	Brooks et al.	341	144	
	AF1	US-6,614,377	09/2003	Adams et al.	341	144	
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Adams, R. <i>et al.</i> , "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," <i>IEEE Journal of Solid-State Circuits</i> 33:12:1879-1886 (December 1998)
	AS	1	Annovazzi, M. <i>et al.</i> , "A Low-Power 98-dB Multibit Audio DAC in a Standard 3.3-V 0.35- μ m CMOS Technology," <i>IEEE Journal of Solid-State Circuits</i> 37:7:825-834 (July 2002)
	AT	1	Baird, R. and Fiez, T., "Improved $\Delta\Sigma$ DAC Linearity Using Data Weighted Averaging," <i>IEEE</i> , pp. 13-16 (1995)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.3750001/RES/GSB	APPLICATION NO. To Be Assigned
	FIRST NAMED INVENTOR Minsheng WANG	
	FILING DATE Herewith (March 31, 2004)	ART UNIT To Be Assigned

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
	AB2						
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FOREIGN PATENT DOCUMENTS

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	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>2</u>	Chen, F. and Leung, B., "Some Observations on Tone Behavior in Data Weighted Averaging," <i>Proceedings of the IEEE 1998 International Symposium on Circuits and System</i> , I-500 through I-503 (May 31 - June 3, 1998)
	AS	<u>2</u>	Chen, K. and Kuo, T., "An Improved Technique for Reducing Baseband Tones in Sigma-Delta Modulators Employing Data Weighted Averaging Algorithm Without Adding Dither," <i>IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing</i> 46:1:63-68 (January 1999)
	AT	<u>2</u>	Fishov, A. et al., "Segmented Mismatch-Shaping D/A Conversion," <i>IEEE</i> , pp. IV-679 through IV-682 (2002)

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	AA3						
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	AJ3						
	AK3						

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	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Folgerman, E. and Galton, I., "A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> 48:3:255-271 (March 2001)
	AS	3	Galton, I., "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," <i>IEEE Transactions on Circuits and System-II: Analog and Digital Signal Processing</i> 44:10:808-817 (October 1997)
	AT	3	Grilo, J. <i>et al.</i> , "A 12-mW ADC Delta-Sigma Modulator With 80dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," <i>IEEE Journal of Solid-State Circuits</i> 37:3:271-278 (March 2002)

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	AA4						
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	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	<u>4</u>	Jensen, H. and Galton, I., "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis," <i>IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing</i> , 45:1:13-27 (January 1998)
AS	<u>4</u>	Kwan, T. <i>et al.</i> , "A Stereo Multibit $\Sigma\Delta$ DAC with Asynchronous Master-Clock Interface," <i>IEEE Journal of Solid-State Circuits</i> 31:12:1881-1887 (December 1996)
AT	<u>4</u>	Norsworthy, S.R. <i>et al.</i> , eds., "Practical Measures for Preventing Idle Tones" in <i>Delta-Sigma Data Converters: Theory, Design and Simulation</i> , IEEE Press, pp. 185-186 (1997)

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	AA5						
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	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	<u>5</u>	Radke, R. et al., "A Spurious-Free Delta-Sigma DAC Using Rotated Data Weighted Averaging," <i>Proceedings of the IEEE 1999 Custom Integrated Circuits Conference</i> , pp. 125-128 (May 16 - 19, 1999)
AS	<u>5</u>	Radke, R. et al., "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging," <i>IEEE Journal of Solid-State Circuits</i> 35:8:1074-1084 (August 2000)
AT	<u>5</u>	Vadipour, M., "Techniques for Preventing Tonal Behavior of Data Weighted Averaging Algorithm in $\Sigma\Delta$ Modulators," <i>IEEE Transactions on Circuits and Systems- II: Analog and Digital Signal Processing</i> , <i>Transactions on Circuits and Systems- II: Analog and Digital Signal Processing</i> 47:11:1137-1144 (November 2000)

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	AA6						
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	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>6</u>	Welz, J. et al., "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," <i>IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing</i> 48:11:1014-1027 (November 2001)
	AS	<u>6</u>	Welz, J. and Galton, I., "A Necessary and Sufficient Condition for Mismatch Shaping in Multi-bit DACs," <i>IEEE</i> , pp. 1-105 through 108 (2002)
	AT	<u>6</u>	Yasuda, A. et al., "A Third-Order Δ - Σ Modulator Using Second-Order Noise Shaping Dynamic Element Matching," <i>IEEE Journal of Solid-State Circuits</i> 33:12:1879-1886 (December 1998)

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	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	<u>7</u>	Zelniker, G. and Taylor, F., "Chapter 7: Multirate Signal Processing" in <i>Advance Digital Signal Processing: Theory and Applications</i> , Marcel Dekker, Inc., New York, NY, pp. 343-361 (1994)
	AS	<u>7</u>	
	AT	<u>7</u>	

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